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EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/531,582	HARADA ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *1-12,18,19 and 22-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-17,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed December 17, 2008.

Claim Objections

1. Claims 13-16, 20 and 21 are objected to because of the following informalities:

In claim 13, “a first conductivity” on lines 4, 27 and 29 should be replaced by “the first conductivity”, “second conductivity” on line 7 should be replaced by “a second conductivity”, “in the lower deposition” on line 9 should be replaced by "of the lower deposition", “in the lower deposition film” should be deleted on line 11, “conductive” on lines 17, 19, 20 and 23 should be replaced by “conductivity”, and “a second conductivity” on line 30 should be replaced by “the second conductivity”.

In claims 14-16, 20 and 21, “a first conductivity” and “a second conductivity” should be replaced by “the first conductivity” and “the second conductivity”.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (US 5,895,939).

Regarding claims 13 and 17, Ueno discloses a silicon carbide semiconductor device (Fig. 3A) (col. 2, lines 66-67) comprising a lower deposition film (bottom layer 32)

(col. 8, line 32) which is formed of a single layer of silicon carbide of a first conductivity type (n-type), and which has lower impurity concentration (n) than a high concentration silicon carbide substrate (n+ substrate) of the first conductivity type (n-type) and which is formed on a surface of the substrate (n+ substrate), a high concentration gate region (40) (col. 8, line 31) of a second conductivity type (p-type) being more heavily-doped (with p-type dopants) (p+) than the lower deposition film (n) (bottom layer 32) and selectively formed in a range from an upper surface of the lower deposition film (bottom layer 32) to an interior of the lower deposition film (bottom layer 32) so as to have a first region (arbitrary region between regions 40) in which low concentration silicon carbide of the first conductivity type (n-type) remains, an upper deposition film (composite layer of 33 and top layer 32) (col. 8, line 37) on the lower deposition film (bottom layer 32), comprising a low concentration gate region (33) of the second conductivity type (p-type) deposited on a surface of the high concentration gate region (40) of the second conductivity type (p-type) and being doped (p) less than the high concentration gate region (p+) (40), a high concentration source region (region denoted as n corresponding to 14 in Fig. 1) (col. 7, line 15) of the first conductivity type (n-type) selectively formed on part of an upper surface of the low concentration gate region (33) of the second conductivity type (p-type) and being more heavily doped *with n-type dopants* than the low concentration gate region (33) of the second conductivity type (p-type), and a low concentration base region (top layer 32) of the first conductivity type (n-type) formed on the first region (arbitrary region between regions 40) and having a second region (whole top layer 32) wider than the first region (arbitrary region between regions 40), a gate

insulation film (36) (col. 8, lines 52-53) formed on at least a surface of the upper deposition film (composite layer of 33 and top layer 32), a gate electrode (G) formed via the gate insulation film (36), a drain electrode (39) (col. 8, lines 35-36) having a low-resistance contact connection with a backside of the silicon carbide substrate (n+ substrate) of the first conductivity type (n-type), and a source electrode (38) (col. 8, line 35) having a low-resistance contact connection with part of the high concentration source region (region denoted as n) of the first conductivity type (n-type) and the low concentration gate region (33) of the second conductivity type (p-type) (claim 13), wherein the upper deposition film (composite layer of 33 and top layer 32) is constituted of silicon carbide (col. 2, lines 66-67) (claim 17).

Ueno differs from the claimed invention by not showing that the low concentration base region of the first conductivity type is doped less than the high concentration source region of the first conductivity type.

It would have been obvious, if not inherent, to the one of ordinary skill in the art at the time the invention was made that the low concentration base region (top layer 32) is doped less than the high concentration source region (region denoted as n), because top layer 32 is an n-type drift layer, which is commonly doped less than a source region which requires heavy doping.

Regarding claims 14 and 16, Ueno further discloses that the low concentration gate region (33) of the second conductivity type (p-type) selectively formed in the upper deposition film (composite layer of 33 and top layer 32) has a portion that is in contact with the gate insulation film (36).

Ueno differs from the claimed invention by not showing that the upper deposition film has a thickness within a range of 0.2 μm to 0.7 μm and wherein the low concentration gate region has an impurity concentration higher than 1×10^{15} cm^{-3} and lower than 5×10^{15} cm^{-3} (claim 14), and an impurity concentration of not higher than 2×10^{16} cm^{-3} (claim 16).

Ueno further discloses a silicon carbide semiconductor device (Fig. 1), wherein a low concentration gate region (top or bottom layer 13) (col. 7, lines 11-13) has a thickness from 1 to 10 μm (col. 7, lines 9-10), and an impurity concentration from 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}.

Since Ueno teaches a silicon carbide semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the thickness of the upper deposition film and the impurity concentration of the low concentration gate region would be about the ranges disclosed by Ueno, because the thickness and impurity concentration can be controlled to achieve a desired device characteristics such as on-resistance and avalanche withstand capability.

Further regarding claims 14 and 16, the claims are prima facie obvious without showing that the claimed ranges of the thickness and impurity concentration achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*,

205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Regarding claim 15, Ueno further discloses for the silicon carbide semiconductor device according to claim 13 that the low concentration base region (top layer 32) of the first conductivity type (n-type) has a lower (p-type) impurity concentration than the high concentration (p+) gate region (40) of the second conductivity type (p-type).

4. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (US 5,895,939) in view of Fukuda et al. (US 2002/0047125). The teachings of Ueno are discussed above.

Regarding claims 20 and 21, Ueno differs from the claimed invention by not showing that in terms of crystal Miller index the surface of the silicon carbide substrate of the first conductivity type is a plane that is parallel to a (11-20) plane (claim 20), or parallel to a (000-1) plane (claim 21).

Fukuda et al. disclose a silicon carbide semiconductor device (Fig. 1), wherein the silicon carbide substrate (1) (lines 1-2 of [0052]) has a (11-20) or a (000-1) surface (claims 17-23) (Please note that (0001) on line 2 of [0052] is a typo of (000-1)).

Since both Ueno and Fukuda et al. teach a silicon carbide semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the silicon carbide substrate disclosed by Ueno may have a (11-20) or (000-1) surface, because these two surface orientations are well-known and commonly

used surface orientations of a hexagonal SiC substrate for fabricating a silicon carbide semiconductor device.

Response to Arguments

5. Applicants' arguments filed December 17, 2008 have been fully considered but they are not persuasive.

Applicants argue that "with such a claimed structure, resistance components from the parts can be reduced and on-resistance can be decreased". Applicants do not specifically claim a resistance of the silicon carbide semiconductor device.

Applicants argue that "Ueno does not disclose or suggest such a claimed structure". As stated in rejection of claim 13, Ueno discloses all the limitations recited n claim 13.

Applicants argue that "such a lower deposition film can, for example, operate as a low concentration n-type drift layer". The Examiner used bottom layer 32 of Ueno as a "single layer lower deposition film", not a composite layer of a bottom layer 32 and a top layer 32 as a "single layer lower deposition film".

Applicants argue that "thereby, not the lower deposition film but the low concentration gate region of the second conductivity type and the low concentration base region are formed on the single layer lower deposition film". Applicants do not specifically claim that the low concentration gate region of the second conductivity type and the low concentration base region are formed **directly** on the single layer lower deposition film. Ueno clearly discloses that the low concentration gate region of the

second conductivity type (33) and the low concentration base region (top layer 32) are formed on the single layer lower deposition film (bottom layer 32).

Applicants argue that "in that respect applicants also note the low concentration base region differs in function from the low concentration lower deposition film". Applicants do not specifically claim functions of the low concentration base region and the low concentration lower deposition film.

Applicants argue that "thereby, Ueno also does not disclose or suggest the above-noted structure". See the above responses.

Applicants argue that "in reply to that statement applicants note in the MOSFET shown in Fig. 3A of Ueno the low concentration p-type layer or gate region is not formed on each of left and right sides of the upper layer-side n-side drift layer". Applicants do not specifically claim whether the low concentration p-type layer or gate region is formed on each of left and right sides of the low concentration base region or not.

Applicants argue that "in contrast to Ueno, as shown in Fig. 4 of the present specification as a non-limiting example, no trench need be formed in the present invention". Applicants do not specifically claim whether a trench is formed or not. Further, it is improper to import claim limitations from the specification. See MPEP 2111.01.

Applicants argue that "the present invention can thereby realize a device having high blocking voltage by the following constitution". Applicants do not specifically claim a device having a high blocking voltage.

Applicants argue that "in such further ways, the present invention differs from Ueno in the function of the p^+ region in the drift layer in the case of applying the reverse voltage". Applicants do not specifically claim a function of the p^+ region.

Applicants argue that "in reply to that grounds for the rejection applicants further note Ueno notes at column 7, lines 11-13 that the layer 13 in Fig. 1 is a "p-type base layer", in contrast the position noted above". The Examiner used Fig. 1 of Ueno to show that the low concentration gate region 33 in Fig. 3 of Ueno may have a certain impurity concentration, not to bodily incorporate the whole structure of Fig. 1 into the silicon carbide semiconductor device shown in Fig. 3A.

Applicants argue that "moreover, the layer 13 shown in Fig. 1 of Ueno does not correspond to the claimed "low concentration gate region of the second conductivity type" (for example, low concentration gate region 11 shown in Fig. 4 of the present specification)", and that "according to the present invention, in contrast, as shown in Fig. 4, the resistance of the current flowing in the low concentration gate region 11 depends on the lateral dimension from the high concentration n^+ source region 5 to the low concentration n^- type base region 4". Applicants do not specifically claim functions of the layers recited in claim 13, and it is improper to import claim limitations from the specification. See MPEP 2111.01.

Applicants argue that "thereby, although both the layer 13 shown in Fig. 1 of Ueno and the low concentration gate region 11 shown in Fig. 4 of the present specification are both p-type semiconductor layers, they completely differ in the function and the influence of the thickness", and that "in such ways the outstanding rejection is

further misconstruing the disclosure in Ueno relative to the claims as written". See the above responses.

Conclusion

6. Applicants' amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
February 3, 2009

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815